28.3 A Per-Pixel Pulse-FM Background Subtraction Circuit with 175ppm Accuracy for Imaging Applications

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In many imaging applications the target is obscured by a large background signal. For example, in infrared (IR) imaging, scenes often have small temperature variations around a much higher background temperature [1]. In noninvasive *in vivo* fluorescence imaging, scenes have high background levels due to tissue autofluorescence caused by the excitation source [2]. Accurately resolving small-signal variations in the presence of a large background signal imposes stringent requirements on the readout circuit, such as necessitating high dynamic range and fine quantization of the total signal. Existing imaging systems mitigate these adverse effects by performing multiple digital read-and-accumulate operations which, as pixel count increases, result in lower sensitivity and longer readout times than the background-limited integration time. Addressing these limitations requires a significant increase in pixel readout area [3].

An alternative approach that overcomes these shortcomings is to perform analog signal subtraction during integration. Since standard AC coupling or differential readout techniques used in other types of sensor interface circuits cannot be used in image sensors, several authors have proposed schemes for per-pixel analog background subtraction [4-8]. The idea is to estimate the background photocurrent every few frames and subtract a large fraction of it from each pixel's photocurrent during integration. The functions needed to estimate the background signal can be readily implemented as part of the standard camera control module (see Fig. 28.3.1). To implement per-pixel subtraction, a current source biased slightly below the background current is added. This current is subtracted from the input photocurrent and the residue is integrated. Such background subtraction relaxes sensor dynamic range requirements, making it possible to reduce the integrating capacitor size and thus pixel area. It can also reduce the ADC resolution and frame rate requirements, and improve sensitivity and linearity. While the shot noise of the subtracted current is added to the photocurrent shot noise, the SNR is improved since the integration time can be increased without saturating the capacitor. It can be shown that background subtraction improves well capacity, SNR and linearity by factors of up to $(1 - \alpha)^{-1}$, $(1 - \alpha^2)^{-1}$ and $(1 - \alpha)$, respectively, where $0 < \alpha < 1$ is the fraction of photocurrent subtracted. The major drawback of current subtraction schemes, however, is high spatial and temporal variations in subtracted current (in the pA to nA range) due to noise and V_t variations.

To surmount these inherent limitations, we propose a per-pixel pulse frequency modulation (PFM) based scheme where charge packets controlled by a PFM signal are subtracted from each pixel's integrator. To validate this scheme, we designed a 1×16 pixel array targeted for bump-bonding with medium and long wave IR HgCdTe diodes (see Fig. 28.3.7). The output of each pixel is connected to a S/H circuit, consisting of a dynamically biased PMOS source follower whose output is connected to a CMOS pass gate and sampling capacitor, followed by an NMOS source follower compensated for its body effect (see Fig. 28.3.2). The S/H allows the output of a pixel with and without background subtraction to be compared in each frame. The array periphery includes bias and timing circuitry and output drivers. The prototype is fabricated in a 0.18μm CMOS 2P5M process and 3.3V thick gate-oxide transistors are used for pixel circuitry.

Each pixel consists of a 30μm×30μm NWELL/PSUB diode (used to simplify characterization) and current source M1 connected to an integrator via switch M2 that is controlled by the PFM signal. The bias current of M1 and the PFM signal pulse-width control the subtracted charge packet size. By selecting a short pulse-width, M1 can be biased at a relatively high level. Its long channel length not only allows operation in strong inversion, which reduces the spatial variations over the array caused by V_t mismatches, but also reduces sensitivity to power supply noise. To achieve high linearity in the subtracted current, only the pulse frequency is varied, with the pulse width and bias current held constant. An alternate current path through M3 is provided when M2 is off to steer the M1 current to node V_B, reducing transients on M1's drain. While V_B should normally be held at the detector node voltage, it is connected to GND instead so that M2 operates in subthreshold, thereby adding a leakage current of around 1pA to emulate the high IR detector dark current. As is common in IR readout circuits, the integrator is a capacitive trans-impedance amplifier (CTIA) implemented with a single-stage telescopic cascode amplifier. Fig. 28.3.3 depicts relevant timing diagrams with the corresponding integrator output.

The minimum current subtracted, around 1.3pA, is limited by the spatial variations of the emulated dark current and corresponds to only one pulse in a 23ms integration time. The maximum current subtracted, around 1μA (M1 bias current), is limited by the CTIA bias. Minimizing GBW variations of the CTIA is critical to reducing subtracted current variations. Although the BW required of the pixel amplifiers is relaxed as in continuous-time ΔΣ schemes, GBW variation causes a variation of the pedestal charge of M2, which is designed to be below 1%.

The prototype has been tested and characterized. Fig. 28.3.6 summarizes chip characteristics and compares performance with and without background subtraction. Fig. 28.3.4 compares measured outputs for pixels with and without background subtraction. The output of the pixel after subtracting 6nA from 6.24nA exhibits a sawtooth pattern due to the periodic charge packet subtraction. Fig. 28.3.5 provides histograms of measured noise and nonlinearity before and after background subtraction for the pixel array with 200pA background photocurrent incremented by twenty 65fA steps. Subtracting 194pA enables the circuit to resolve a signal hidden within the background with an accuracy of 175ppm at 43frames/sec with a 30-fold increase in effective well capacity. Linearity improvement is less than the theoretically achievable value of 4fA due to the integrator INL, since the signal of interest now spans the entire range of the integrator. Furthermore, measurement accuracy is also limited by the light source nonlinearity. Measured peak spatial subtracted current variation over the array is 3%. Temporal and spatial variations reported are at least 17 and 5 times lower, respectively, than that obtained by subtracting the background by controlling the M1 bias current as in [6]. Since variations in the PFM pulse-width directly affect the charge packet size, linearity and current variations can be further improved by generating the PFM signal on chip (instead of externally as in this work). The paper described a 1-D array design. Given the low pixel overhead of our scheme, a 2-D array can be readily designed.

Acknowledgements:
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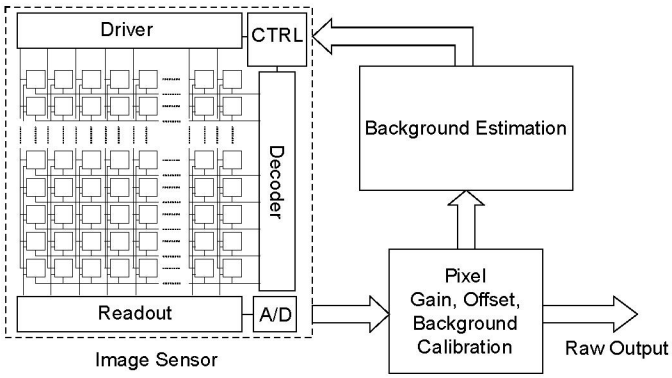

Figure 28.3.1: Imaging system with background subtraction.

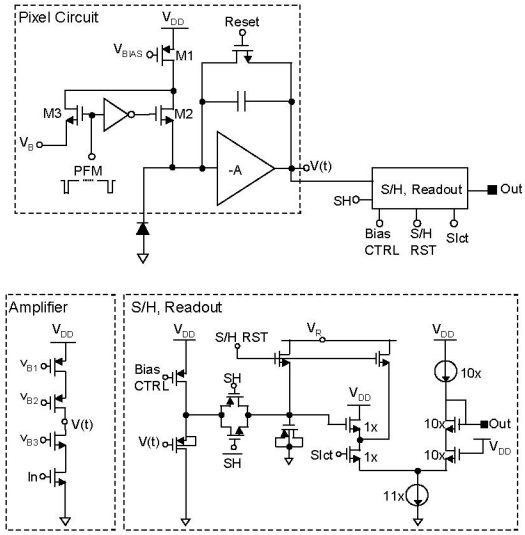

Figure 28.3.2: Pixel schematic for PFM background subtraction scheme.

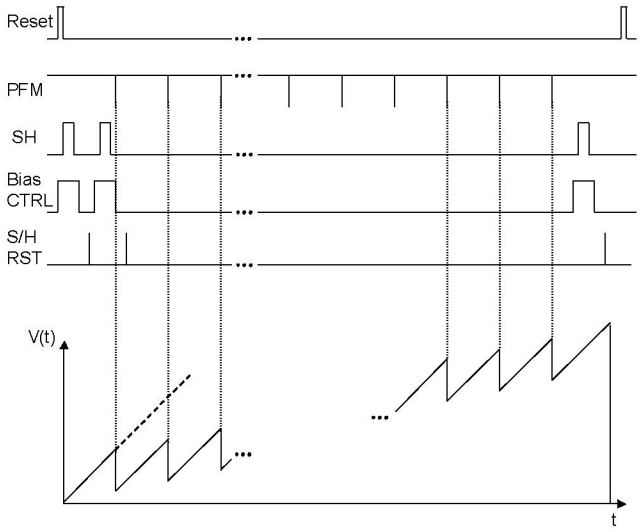

Figure 28.3.3: Timing diagram and corresponding integrator output.

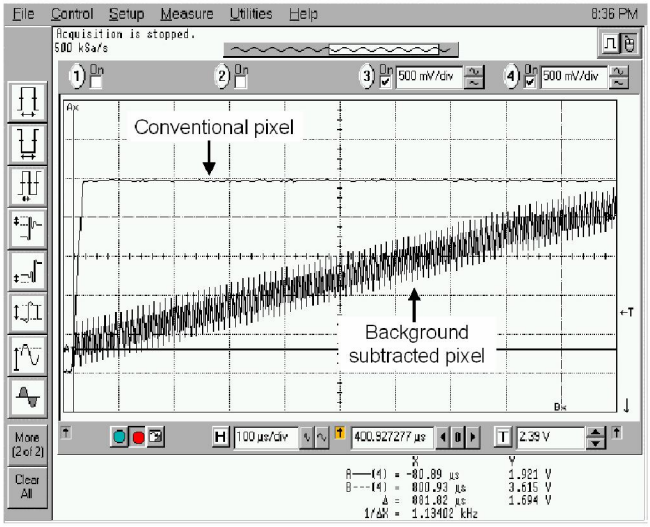

Figure 28.3.4: Plot of outputs for pixels with and without background subtraction.

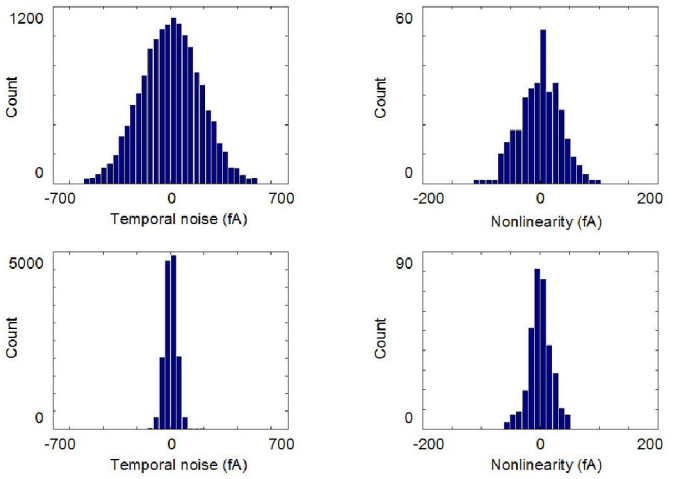

Figure 28.3.5: Histograms of measured noise and nonlinearity for the pixel array with conventional readout (top) and with background subtraction (bottom).

Chip characteristics	
Technology	0.18µm CMOS
Array size	16×1
Pixel circuit area	900µm^2
NWELL/PSUB diode area	900µm^2
Emulated dark current	1pA
Minimum integration time	1µs
Integrator capacitance	100fF
Integrator voltage swing	1.5V
CTIA gain	69dB
Readout DNL	0.15%
Pixel power consumption	19µW

Performance comparison	Conventional	Background subtracted
Effective well capacity	937,500 e$^-$	28,218,750 e$^-$
Integration time	766µs	23ms
Maximum photocurrent	200pA	6pA (α=0.97)
Subtracted current	0	194pA
Peak SNR	60dB	75dB
Temporal noise standard deviation	176fA	35fA
Maximum nonlinearity	104fA	54fA
Background subtraction spatial variation	N/A	3% peak

Figure 28.3.6: Chip characteristics and measured performance comparison.

Continued on Page 618

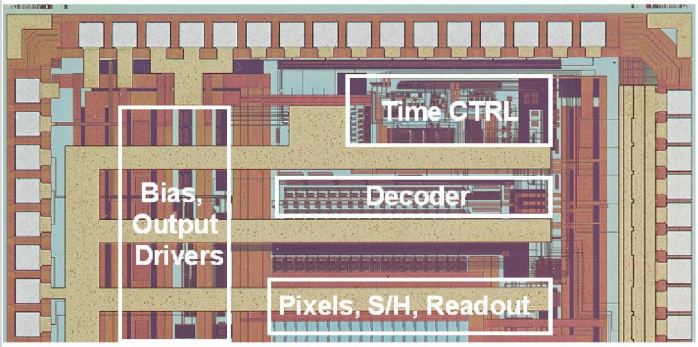

Figure 28.3.7: Chip micrograph.

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